

FPGAs in radiation-harsh environments



Application examples

AFDX

- ◆ Used on new commercial aircrafts from Boeing and Airbus
- ◆ Main communication interface
- ◆ Safety level up to DAL-A



Mission computers

- ◆ Used on all aircrafts
- ◆ e.g. freight control system for Airbus A400M
- ◆ Safety level up to DAL-A



The old Style: ARINC-429

ARINC-429 commonly found in aircrafts of the 80s

- ◆ Mono directional bus → 1 transmitter, $n \leq 20$ receivers
- ◆ Dedicated wiring for each connection
- ◆ 100s km cabling per aircraft
- ◆ Transmission rates: 100kbit/s and 14.5kbit/s (low critical)



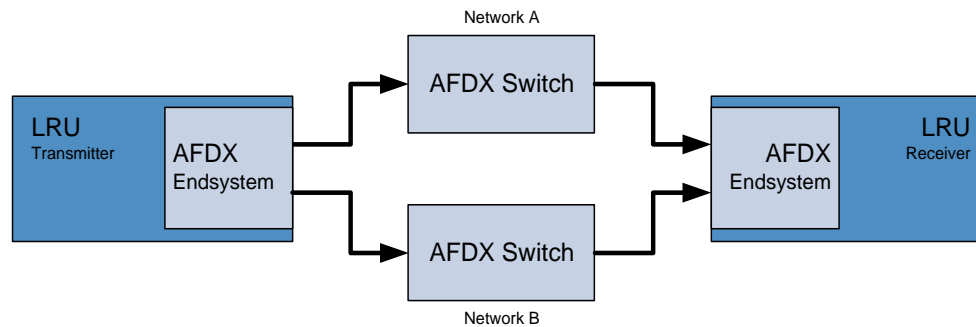
Nowadays: AFDX Technology

Based on IEEE802.3 Ethernet

- ◆ 100Mbit/s Ethernet
- ◆ Full duplex
- ◆ Switched
- ◆ Full static configuration, no ARP, no DNS, ...

Provides Reliable Data Transport

- ◆ Known latency
- ◆ High availability through redundancy

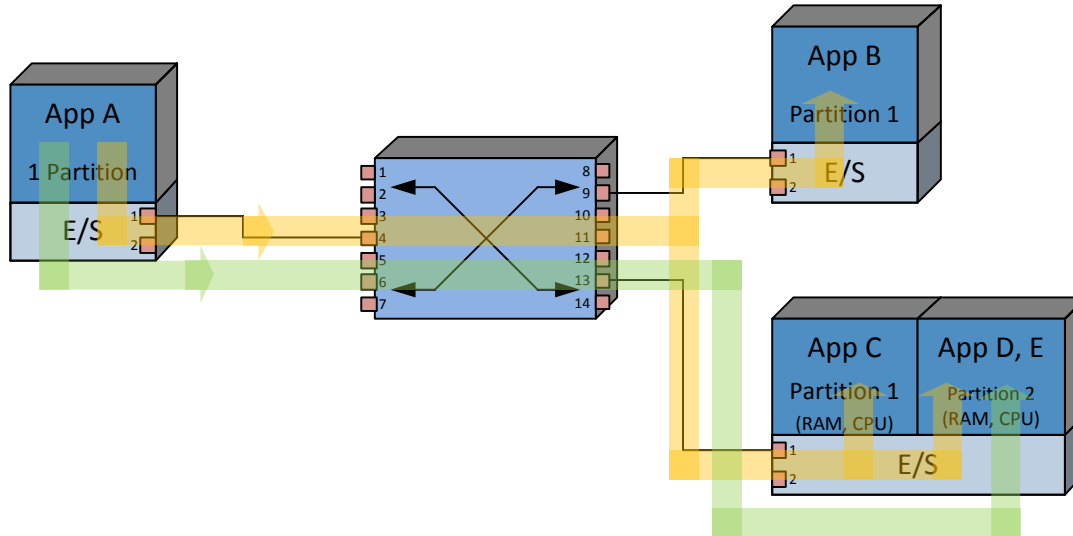


Redundant Network Architecture

AFDX – Virtual Links replace ARINC-429

Avionics communications are based on multicast

- ◆ One transmitter
- ◆ One or several receivers

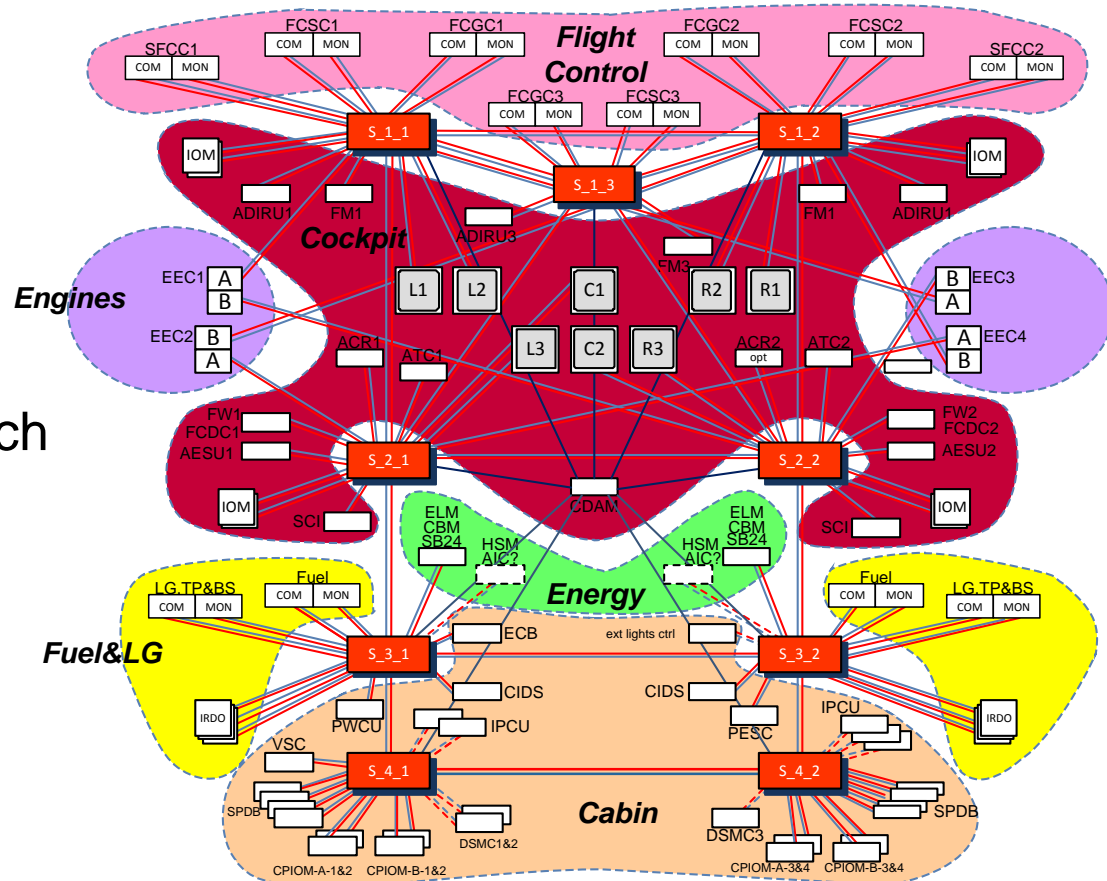


⇒ *Virtual links provide similar properties as ARINC-429*

Airbus A380: AFDX Network

A380 AFDX network

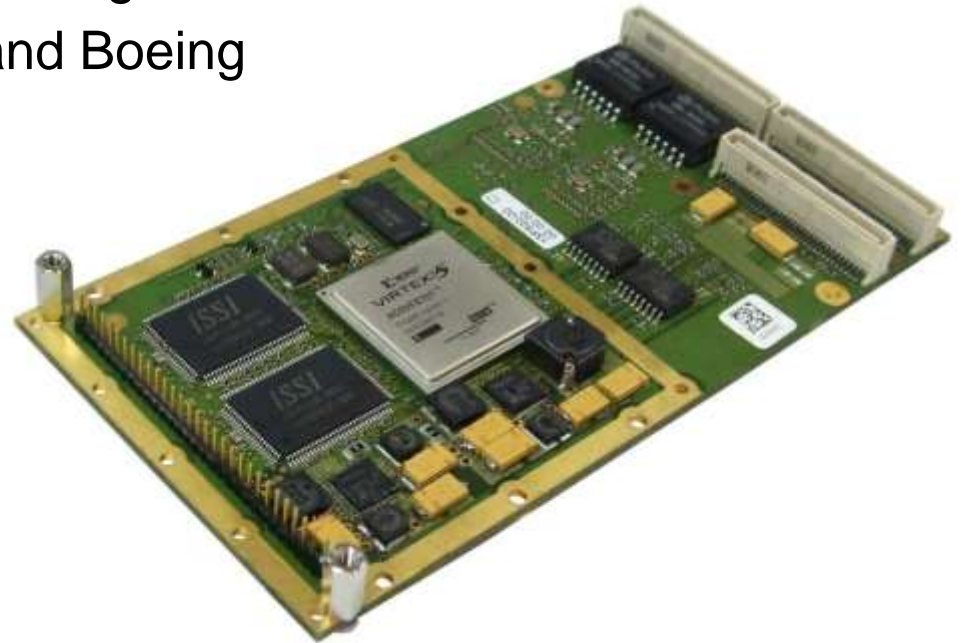
- ◆ 100Mbit/s Ethernet
- ◆ Redundant networks (A&B)
- ◆ AFDX switches (2 x 9)
- ◆ #of ports on each switch (20 – 24)
- ◆ Up to 80 AFDX end-systems



AFDX – Ethernet for Mission-Critical Applications

AFDX interface

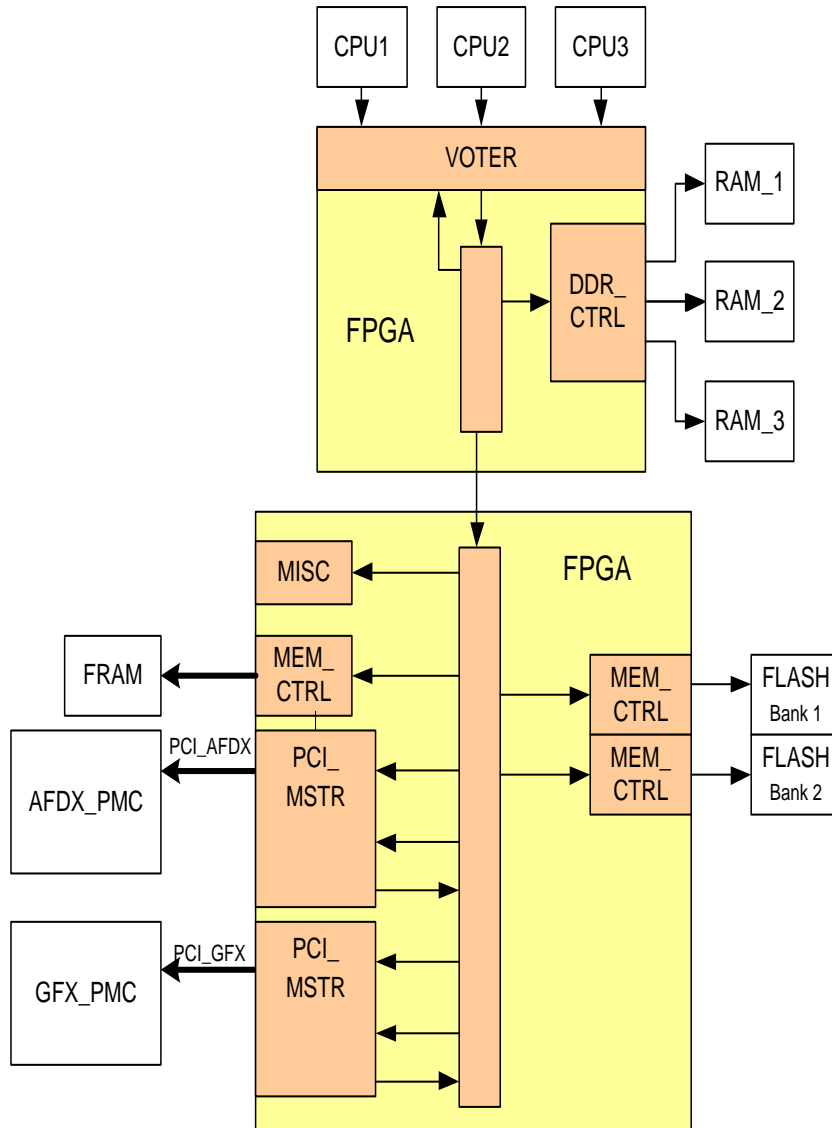
- ◆ Certifiable FPGA implementation
- ◆ Available on PMC P520
- ◆ Full-featured AFDX protocol engine
- ◆ Interoperable with Airbus and Boeing



Airbus A400M Freight System



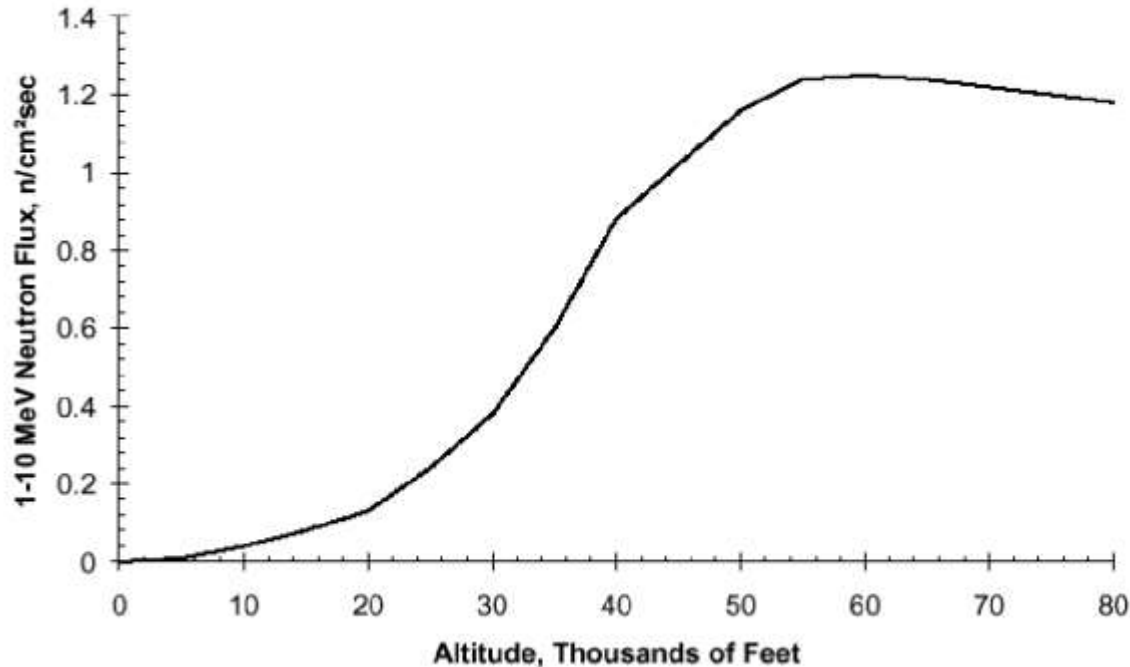
Mission Computer with FPGA Architecture



- ◆ Triple redundancy on board
- ◆ 3x redundant PowerPC 750 CPU with up to 800 MHz (Lockstep)
- ◆ Redundant memory
- ◆ Onboard data transfers paths realized with FPGAs
- ◆ Voting done inside FPGA
- ◆ Compliant with DO-254 up to DAL-A

Challenge: Single Event Upsets/Multi Bit Upsets

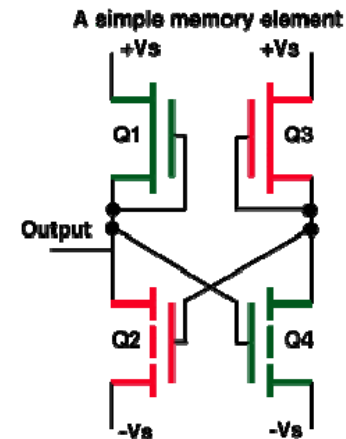
- ◆ Aircrafts are exposed to radiation environment
- ◆ Neutrons (Secondary Cosmic Ray Particles) may cause SEUs and MBUs in electronics equipment
- ◆ Particle flux varies with altitude - max. flux at 60.000 ft.



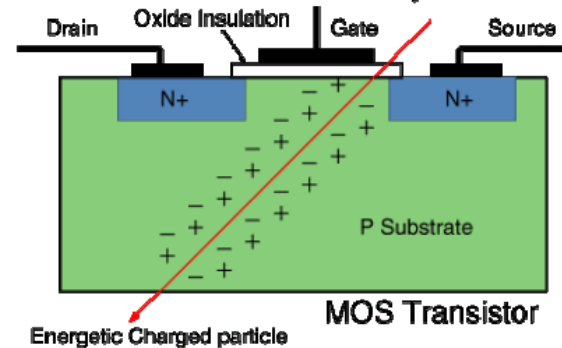
SEU/MBU Effects

Components susceptible to SEU/MBU bit flips

- ◆ SRAMs
- ◆ SDRAMs
- ◆ Microprocessors
 - Register
 - Caches
 - Internal buffers/FIFOs
- ◆ FPGAs
 - Cell configuration
 - Logic cell state
- ◆ ...



Interaction of a Cosmic Ray and Silicon



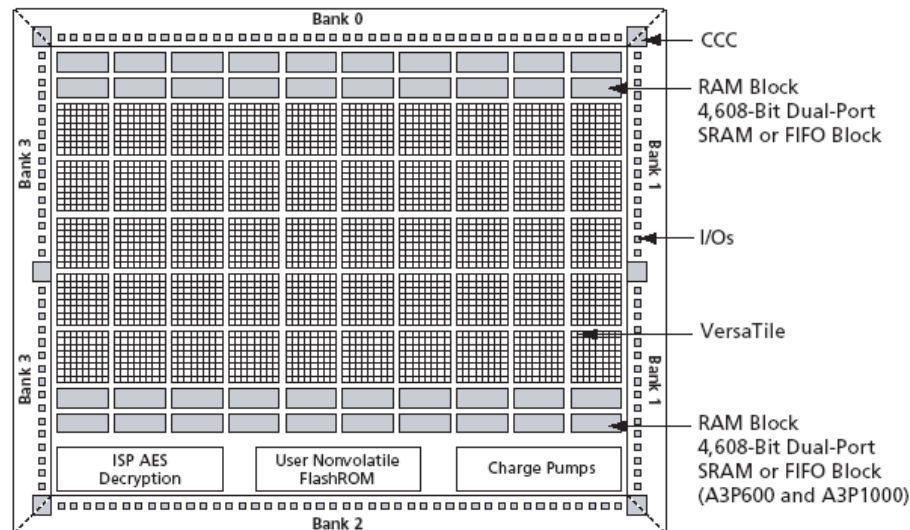
FPGA Issues

FPGA configuration must be SEU hardened

- ◆ FPGAs with RAM based configuration need mitigation strategy
- ◆ FPGAs with FLASH based configuration are SEU/MBU immune

But

- ◆ Registers and RAM within FPGAs still not SEU immune!
- ◆ Other mitigation techniques required



SEU/MBU RAM Sensitivity

Failure probability 10^{-7} / flight-hour (DAL B)

- ◆ Only one safety relevant failure in 10 Mio. flight hours!

Error probability increases with number of bits

Examples

- ◆ 512MByte SDRAM at 60.000 ft. (no ECC)

→ Fails after 10 hours!

- ◆ 32kByte cache

→ Fails after 3.5 month

⇒ *Safe airplanes would not be possible*

Architectural Solutions

Register and logic protection strategies

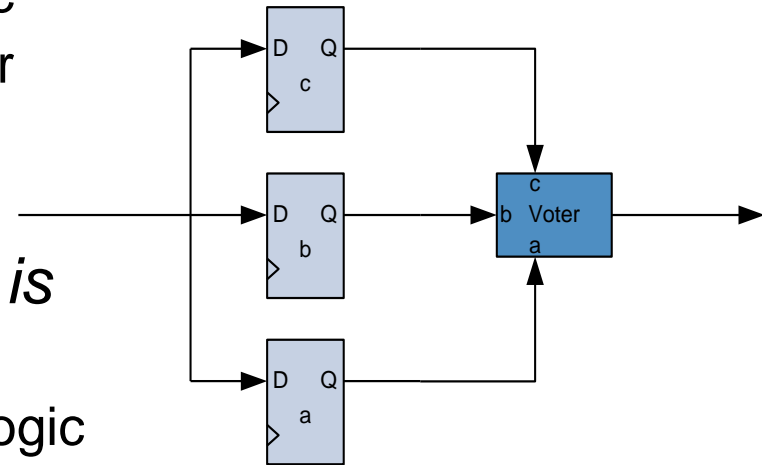
- ◆ All FPGA registers subject to SEUs
- ◆ Critical sections use 2oo3 voting logic
- ◆ Majority voter overrules faulty register value

Triple modular redundancy (TMR) is expensive

- ◆ Requires more than 3 times regular logic
- ◆ Slows down timing up to 20%

TMR significantly lowers the probability of SEU induced failures in the FPGA logic

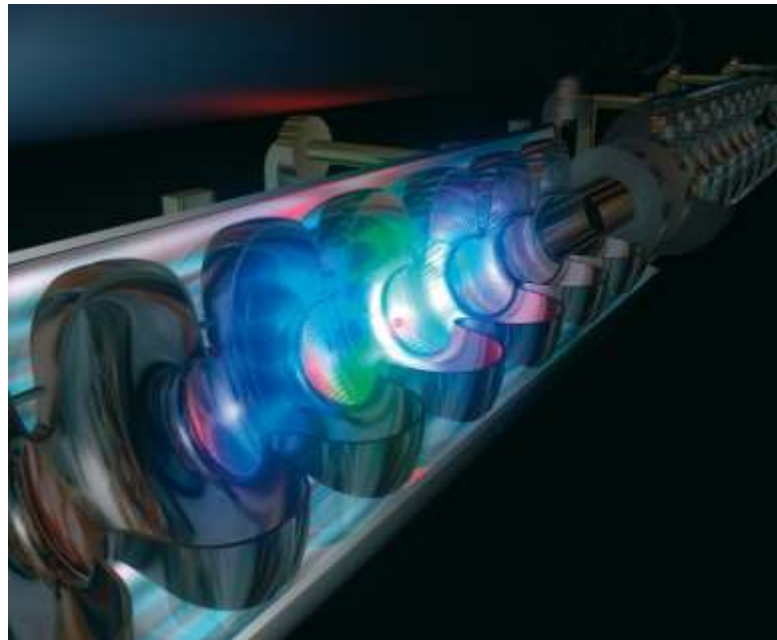
⇒ Safe airplanes are possible



Verification of TMR Technology

Architectural mitigation strategy can be verified by proton beam experiments

- ◆ DUT is exposed to particle beam with density equivalent to high altitude radiation
- ◆ DUT is running in test to demonstrate operability



Source: http://xfel-development.4pi-communications.net/media/assets/XFEL_Beschleuniger02-jpg

Thank you for your attention!

Embedded Solutions

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Mobile and Mission-Critical Environments*



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