

Michael Munroe
Elma Electronic Inc.

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The Compliance Challenge?



Protocols used by VITA 65

Protocol	Data Rate
1000Base-KX	1.25
PCIe 1.1	2.5
PCIe 2.1	5.0
SRIO 1.3	3.125
SRIO 2.1	5.0
SRIO 2.2	6.25
10GBase-KX4	3.125
PCIe 3.0	8/32
10GBase-KR/KR4	10/40
InfiniBand FDR	14/56
Ethernet 802.3bj	25.0 (May 2014) ?



- Ethernet, sRIO and PCIe products with 2.5, 3.125, 5, and 10 Gbaud channels too numerous to mention
- sRIO DDR backplanes (6.25 and 25 Gbaud channels)
- sRIO DDR daughter cards (6.25 and 25 Gbaud channels)
- PCIe Gen 3 backplanes (8, 16 and 32 Gbaud channels)
- PCIe Gen 3 daughter cards (8, 16 and 32 Gbaud channels)
- IEEE 802.3ba backplane (10 and 40 Gbaud channels)
- IEEE 802.3ba daughter cards (10 and 40 Gbaud channels)
- InfiniBand FDR daughter cards (14 and 64 Gbaud channels)



- Demonstrating that products work together is no guarantee that they will work together in another system unless there are channel requirements and agreed upon methods for assessing compliance.
- True interoperability means that daughter cards from different vendors can interoperate in backplanes by a third party integrated by someone else.

6.4 Backplane compliance criteria:

It is straightforward to map the IEEE 802.3-2008 model onto VPX to establish criteria for the whole channel. **Once that is done, we need to establish the compliance points for the backplane portion, and allocate a portion of the total budget for each parameter to the backplane.** Table 6.4-1 below establishes the budget for allocating the IEEE 802.3-2008 parameters to the backplane and defers the Tx and Rx allocations in the dot specs. Refer to Section 6.3 and Figure 6.3-1 above for the VPX compliance channel definitions.

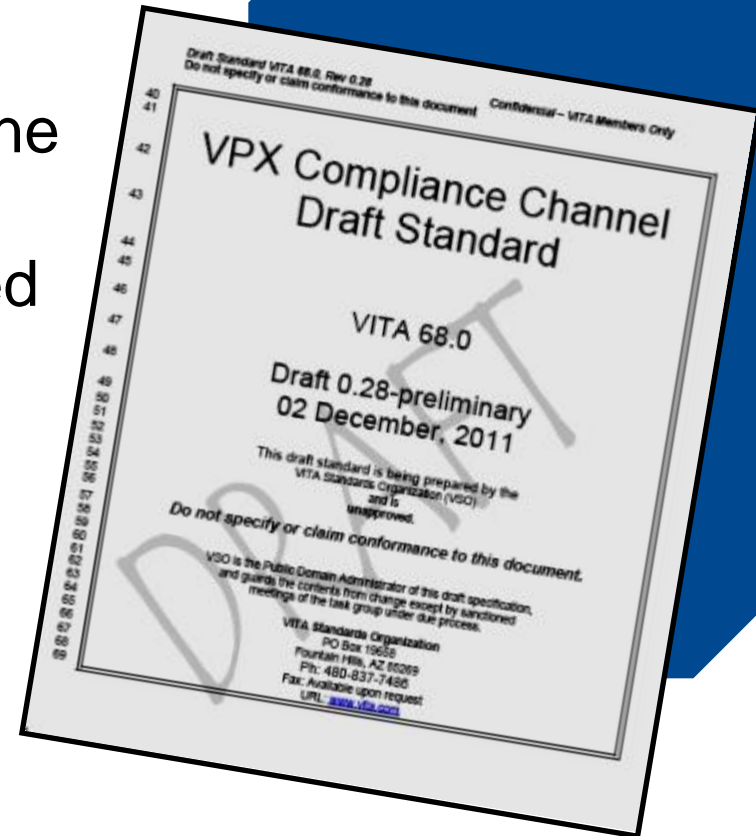


How do we ensure boards interop?

Demonstrating that products work together is no guarantee that they will work together in another system unless there are channel requirements and accepted procedures for assessing compliance.



- VITA 68 intends to support all Open VPX speeds and protocols
- But it is not complete and no one has signed up to fund the simulation to define the required compliance fixtures



Major Channel Efforts

Standard	Data Rate	Completion	Effort
IEEE 802.3ba	10/40 Gbps	May 2012	30 months
PICMG 3.1R2	10/40 Gbps	August 2012	55 months
PICMG Exp0R2	8 GTps	May 2013	28 months
VITA 68 for 65	Up to 10 Gbps	pending	50 months
VITA 802.3bj	25/100 Gbps	May 2014	18* months

*Note that this short 18 month process was only possible because the group built on 802.3ba.



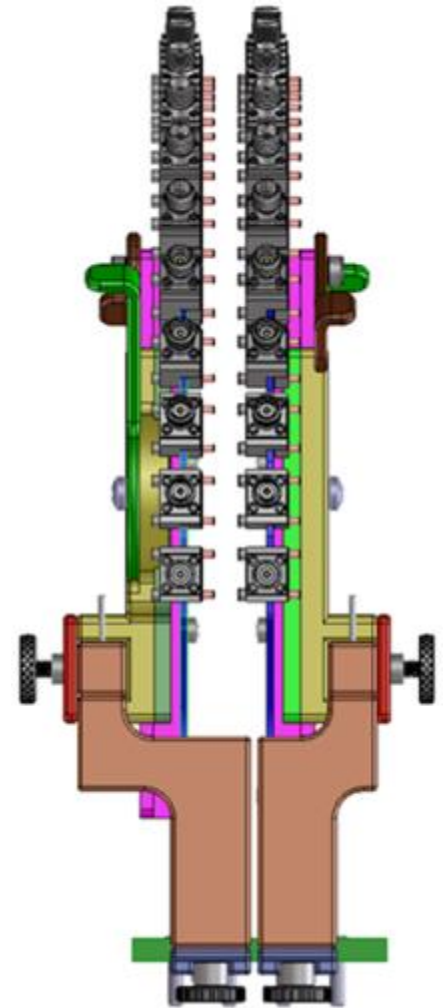
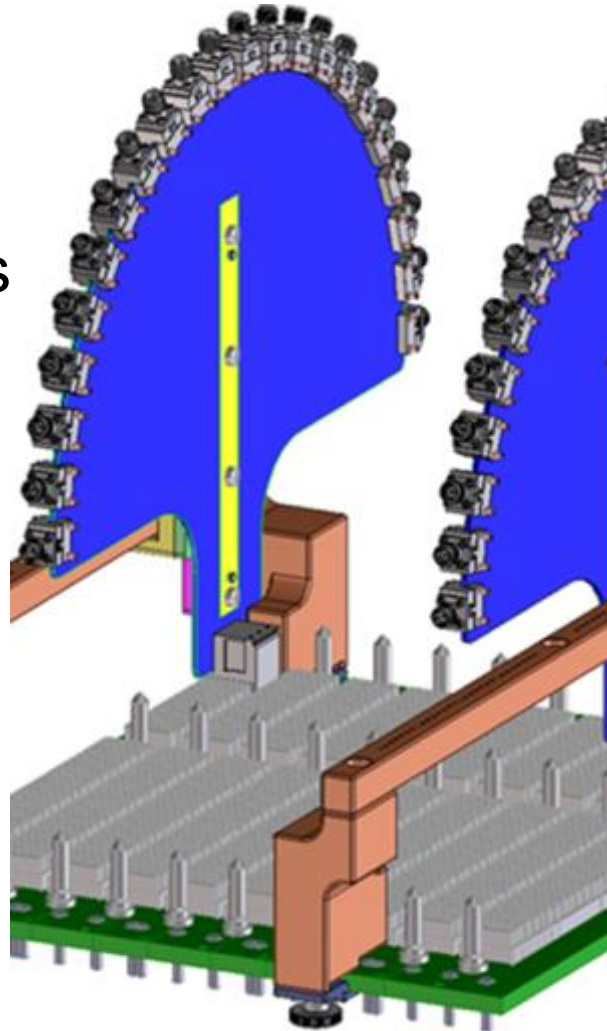
What can be done?

- Board are already using Megtron6
- Back-drilling is being done to industry capability
- Layout has challenged the tightest available tolerances for layer to layer registration.
- Changing the basic footprint would be essentially be a new architecture.
- Connector tweaks – vias, blocking capacitors

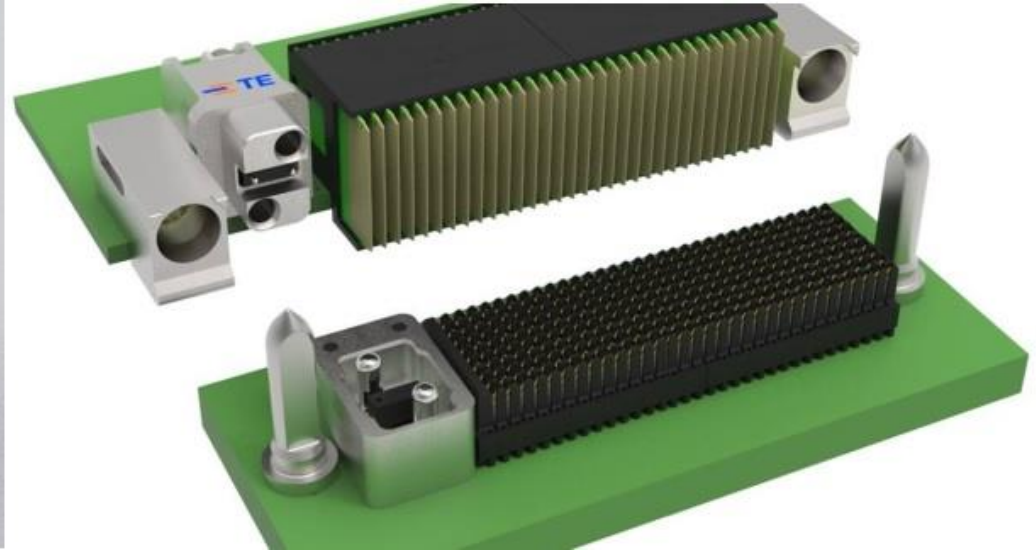
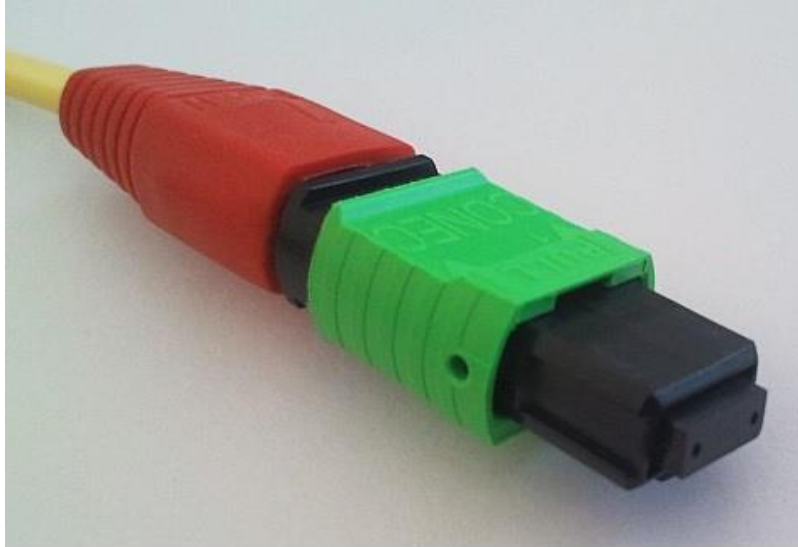


Compliance takes work

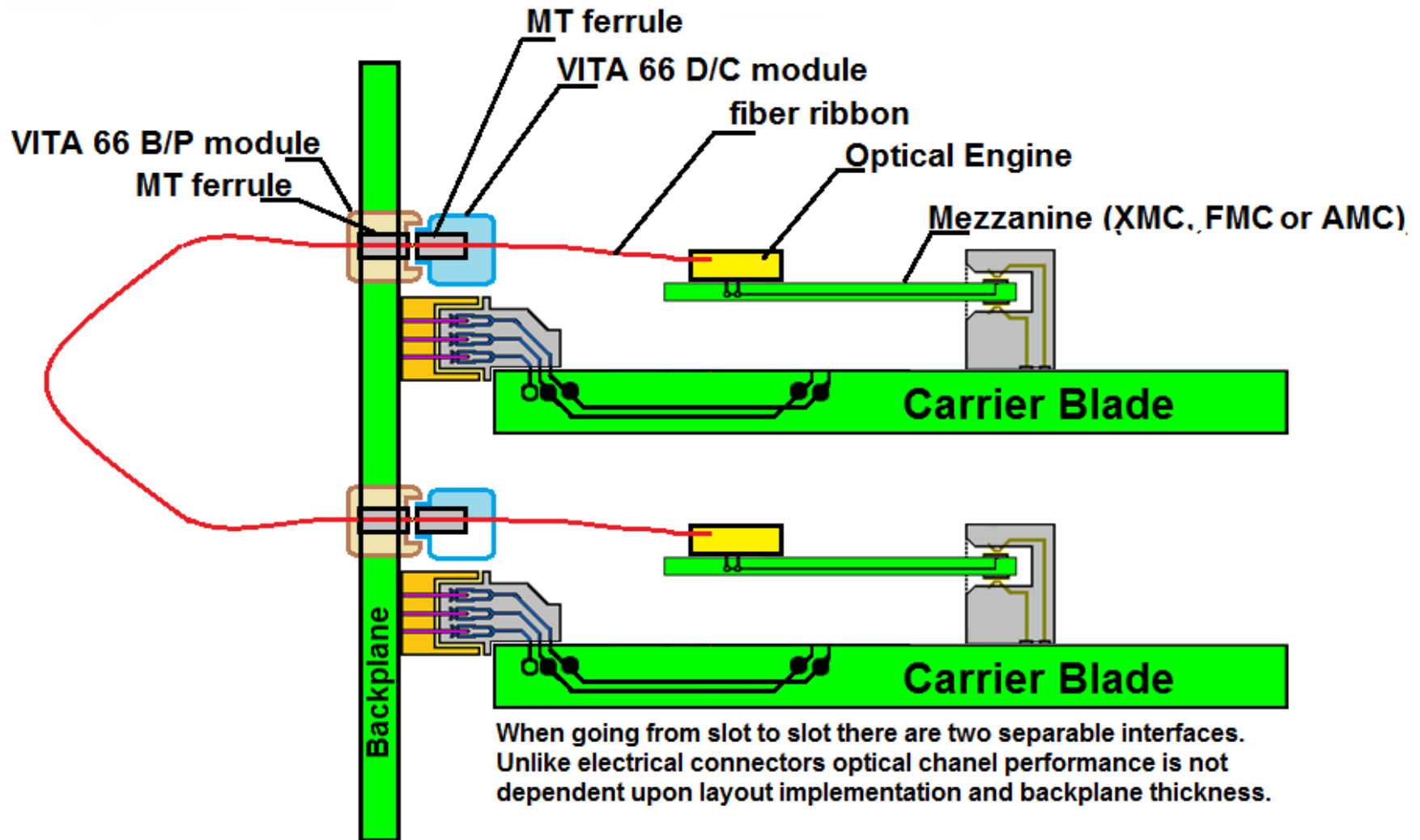
We need simulations validated by measurements and documented procedures for implementation.



VITA 66.4 Components



VITA 66.4 Implementation

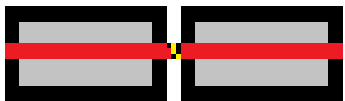
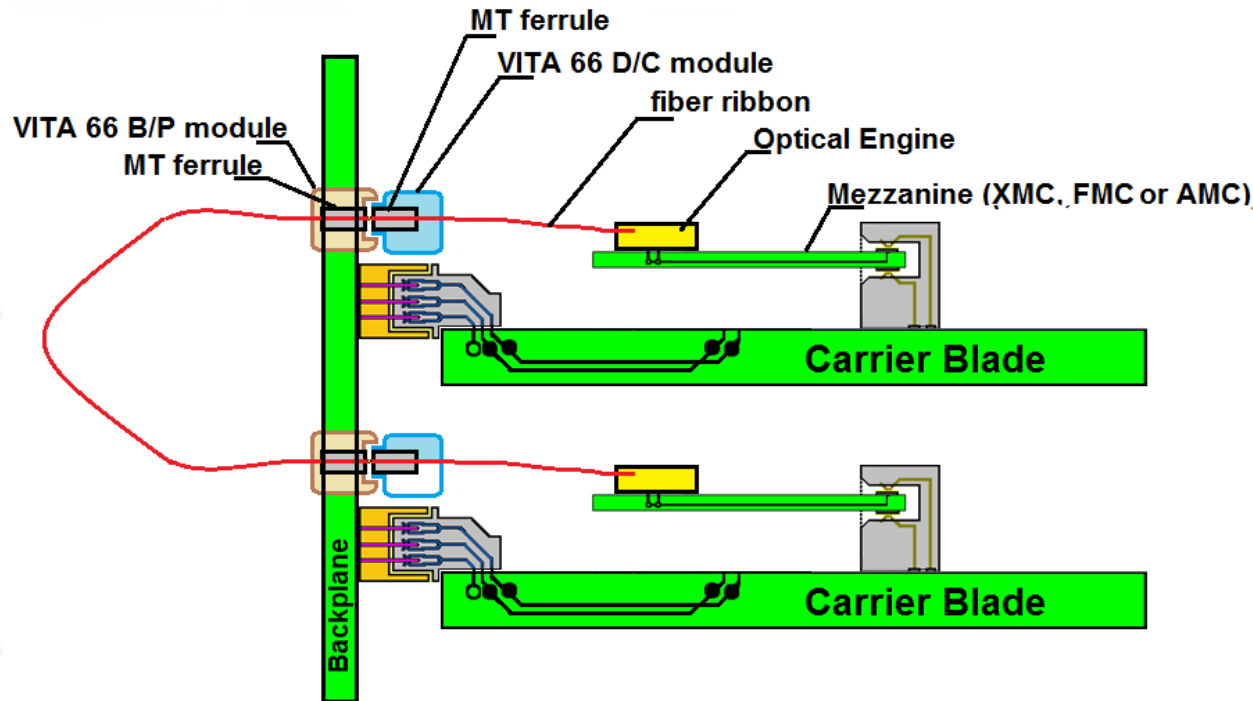


VPX Optical Extensions

Protocol	Data Rate (Cu)	Optical	
		4x	12X
PCIe 3.0	8/32		
10GBase-KR/KR4	10/40		
InfiniBand FDR	14/56	14/56	14/168
Ethernet 802.3bj	25.0 (May 2014) ?	25/100	25/300
InfiniBand EDR			25/300
InfiniBand HDR			50/600



VITA 66 Optical on VPX



MT Interface

The MT ferrule supports up to 24 optical fibers (in ribbons of 12 fibers)
Ferrules have been produced supporting 5 rows of 12.



Thank You For Your Time

Michael Munroe
Elma Electronic, Inc.
michael.munroe@elmabustronic.com

www.elma.com
sales@elma.com

